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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,724	10/25/2001	Ruben P. Madrid	TI-27987	2847

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EXAMINER

MALDONADO, JULIO J

ART UNIT PAPER NUMBER

2823

DATE MAILED: 12/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/002,724

Applicant(s)

MADRID ET AL.

Examiner

Julio J. Maldonado

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2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 25 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) 14-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments, see page 2, filed on 08/25/2003, with respect to the rejection(s) of claim(s) 1 and 8 under 35 USC §103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Exposito et al. (U.S. 6,087,202) and Glenn et al. (U.S. 2002/0168798 A1).

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 4, 5, 7, 8, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Exposito et al. (U.S. 6,087,202) in view of Glenn et al. (U.S. 2002/0168798 A1).

In reference to claims 1 and 8, Exposito et al. (Figs.1-9) in a related method to form a plurality of ball grid array teach providing a plurality of chips (103); coupling the chips (103) to a first side of a substrate (102); attaching a plurality of solder balls (107) to a second side of the substrate (102); and cutting the substrate to produce the ball grid array (column 2, line 35 – column 3, line 53).

Exposito et al. fail to teach the plurality of chips comprise a flip chips. However, Glenn et al. (Figs.1, 2 and 20-22) in a related method to form a plurality of ball grid array

packages teaches providing a plurality of flip chips (10A); and coupling the flip chips (10A) to a first side of a substrate (12) ([0053], [0111] – [0115] and [0131]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Exposito et al. and Glenn et al. to enable forming the chips of Exposito et al. as taught by Glenn et al.

In reference to claims 4 and 10, the combined teachings of Exposito et al. and Glenn et al. teach wherein coupling the flip chip to the first side of the substrate comprises soldering a plurality of solder bumps coupled to the flip chip to a plurality of solder pads on the first side of the substrate (Glenn et al., [0114]).

In reference to claims 5 and 11, the combined teachings of Exposito and Glenn et al. teach wherein encapsulating the flip chip with the molding comprises encapsulating the flip chip by utilizing a transfer molding process (Glenn et al., [0131]).

In reference to claim 7, the combined teachings of Exposito et al. and Glenn et al. teach wherein cutting the substrate comprises cutting the substrate in a first direction; and after cutting the substrate in the first direction cutting the substrate in a second direction substantially perpendicular to the first direction (Exposito et al., Figs.7 and 9).

4. Claims 2, 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Exposito et al. (U.S. 6,087,202) in view of Glenn et al. (U.S. 2002/0168798 A1) as applied to claims 1, 4, 5, 7, 8, 10 and 11, above, and further in view of Glenn et al. (U.S. 6,309,943 B1).

The combined teachings of Exposito et al. and Glenn et al. substantially teach all aspects of the invention teach wherein the plurality of flip chips comprises forming a plurality of integrated circuit dies on a wafer, and coupling a plurality of solder bumps to the integrated circuit dies (Exposito, Fig.8, column 1, lines 14 – 21, and column 3, lines 43 – 46). The combined teachings of Exposito et al. and Glenn et al. fail to teach scribing the wafer to define edges of the flip chip; and transferring the ball grid array package to a shipping tray. However, Glenn et al. (Fig.1) in a related method form a packaging structure teach a wafer (10) with integrated circuits (12), and scribing the wafer (10) to define edges of the circuit array (column 1, lines 15 – 25). Glenn et al. also teach (in Fig.9) after forming the packaging structure, transferring said structure to a shipping tray (column 12, lines 36 – 46). Therefore, it would have been obvious to combine the teachings of Glenn et al. with the teachings of Exposito et al. and Glenn et al. to enable scribe lines on the wafer to define edges of the flip chip, and transferring the ball grid array to a shipping tray as taught by Glenn et al.

5. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Exposito et al. (U.S. 6,087,202) in view of Glenn et al. (U.S. 2002/0168798 A1) as applied to claims 1, 4, 5, 7, 8, 10 and 11, above, and further in view of Tani et al. (U.S. 6,410,363 B1).

Exposito et al. in combination with Glenn et al. substantially teach all aspects of the invention but fail to teach wherein encapsulating the flip chip with the molding comprises encapsulating the flip chip with an epoxy. However, Tani et al. in a related method to form a package structure teach a conventional encapsulating process

including encapsulating a chip with a molding comprising an epoxy (column 1, lines 30 – 45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Exposito et al. and Glenn et al. with the teachings of Tani et al. to enable using epoxy in the embodiment as taught by Exposito et al. and Glenn et al. as taught by Tani et al.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Exposito et al. (U.S. 6,087,202) in view of Glenn et al. (U.S. 2002/0168798 A1) as applied to claims 1, 4, 5, 7, 8, 10 and 11, above, and further in view of Akram et al. (U.S. 6,423,616 B2).

The combined teachings of Exposito et al. and Glenn et al. substantially teach all aspects of the invention but fail to show cutting the substrate in a first direction with a plurality of cutting blades; rotating the substrate substantially 90 degrees with respect to the cutting blades; and cutting the substrate in a second direction substantially 90 degrees to the first direction. However, Akram et al. (Figs.3-5) in a related method to singularize a plurality of semiconductor chip from a substrate teach cutting said substrate (52) in a first direction with a plurality of cutting blades (32, 34); rotating a substrate (52) substantially 90 degrees with respect to the cutting blades (32, 34); and cutting the substrate (52) in a second direction substantially 90 degrees to the first direction (column 4, line 10 – column 5, line 40). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Exposito et al. and Glenn et al. with the teachings of Akram et al. to enable cutting the substrate of Exposito et al. and Glenn et al. as taught by Akram et al., and

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furthermore, since this would increase the speed of cutting the substrate (column 3, lines 1 – 3).

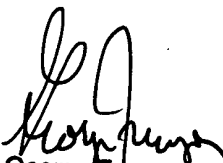
### **Conclusion**

7. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via [julio.maldonado@uspto.gov](mailto:julio.maldonado@uspto.gov). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

  
JMR  
11/18/03

  
George Faurson  
Primary Examiner